CLAIMS

1. A method of designing a memory device that has reduced bitline capacitance offsets; comprising:

providing a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline;

designing a core cell having a bitline and a complementary bitline;

designing a flipped core cell that has a flipped bitline and a flipped complementary bitline; and

arranging the core cell followed by the flipped six transistor core cell along each of the multiple pairs of the global bitline and the global complementary bitline.

2. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the bitline of the core cell is coupled with the flipped complementary bitline of the flipped core cell, and the complementary bitline of the core cell is coupled to the flipped bitline of the flipped core cell.

3. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 2, further comprising:

coupling successive pairs of the core cell and the flipped core cell along each of the multiple pairs of the global bitline and the global complementary bitline.

4. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the designing of the flipped core cell includes:

flipping the core cell horizontally about a Y-axis that is defined at a rightmost edge of the core cell to produce an intermediately flipped core cell; and

flipping the intermediately flipped core cell vertically about an X-axis that is defined at a lowermost edge of the intermediately flipped core cell to produce the flipped core cell.

5. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 4, wherein the bitline of the core cell is coupled with the flipped complementary bitline of the flipped core cell, and the complementary bitline of the core cell is coupled to the flipped bitline of the flipped core cell.

6. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 5, further comprising:

coupling successive pairs of the core cell and the flipped core cell along each of the multiple pairs of the global bitline and the global complementary bitline.

7. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 2, wherein the bitline has a first capacitance and the complementary bitline has a second capacitance.

8. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 7, wherein the flipped bitline the first capacitance and the flipped complementary bitline has the second capacitance.

9. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 8, further comprising:

achieving an equal capacitance on the global bitlines and the global complementary bitlines when the bitline of the core cell is coupled with the flipped complementary bitline of the flipped core cell, and the complementary bitline of the core cell is coupled to the flipped bitline of the flipped core cell.

10. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the memory device is fabricated onto a semiconductor chip.

11. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 1, wherein the memory device is designed using a memory generator.

12. A method of designing a memory device that has reduced bitline capacitance offsets ina memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline, comprising:

providing a core cell having a bitline and a complementary bitline;

providing a flipped core cell that has a flipped bitline and a flipped complementary bitline; and

arranging a plurality of the core cell in a column and a plurality of the flipped core cell in the column, such that the plurality of the core cell equals the plurality of the flipped core cell.

13. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 12, wherein the plurality of the core cell and the plurality of the flipped core cell are aligned in the column that corresponds to the multiple pairs of the global bitline and the global complementary bitline.

14. A method of designing a memory device that has reduced bitline capacitance offsets as recited in claim 12, wherein a memory generator is used for designing the memory device.